Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

1. (Currently Amended) A decoder for demodulating address information using a wobble signal, the decoder comprising:

a digital PLL circuit for generating a first clock signal and synchronizing the first clock signal with the wobble signal based on a difference between the phase of the wobble signal and the phase of the first clock signal;

an analog PLL circuit for generating a second clock signal and synchronizing the second clock signal with the wobble signal based on a difference between the phase of the wobble signal and the phase of the second clock signal; and

a demodulator, connected to the digital PLL circuit and the analog PLL circuit and configured to be able to switch between the first and second clock signals, [[~~for~~]] the demodulator sampling the wobble signal using either the first clock signal or the second clock signal to demodulate the address information~~, wherein the demodulator samples the wobble signal using the first clock signal until the second clock signal is synchronized with the wobble signal and samples the wobble signal using the second clock signal after the second clock signal is synchronized with the wobble signal~~.

2. (Previously Presented) The decoder as claimed in claim 1, further comprising a detection circuit for comparing the wobble signal and the second clock signal and detecting whether the second clock signal is synchronized with the wobble signal, wherein the demodulator selects either sampling the wobble signal using the first clock signal or sampling the wobble signal using the second clock signal based on a detection result of the detection circuit.

3. (Original) The decoder as claimed in claim 2, wherein the analog PLL circuit includes:

a phase comparator for generating a phase difference signal in response to a difference between the phase of the wobble signal and the phase of a divisional clock signal generated by dividing the frequency of the second clock signal by a predetermined frequency dividing ratio;

a charge pump, connected to the phase comparator, for generating current in accordance with the phase difference signal;

a low pass filter, connected to the charge pump, for generating voltage in accordance with the current of the charge pump; and

a voltage-controlled oscillator, connected to the low pass filter, for oscillating in accordance with the voltage of the low pass filter and generating the second clock signal, wherein the detection circuit compares the wobble signal and the divisional clock signal and detects whether the second clock signal is synchronized with the wobble signal.

4. (Cancelled)

5. (Original) The decoder as claimed in claim 1, wherein the demodulator includes:

a first phase detector, connected to the digital PLL circuit, for detecting a phase inversion of the wobble signal based on the first clock signal; and

a second phase detector, connected to the analog PLL circuit, for detecting a phase inversion of the wobble signal based on the second clock signal.

6. (Original) The decoder as claimed in claim 5, wherein the demodulator includes a selector, connected to the first and second phase detectors, for selecting either the detected result of the first phase detector or the detected result of the second phase detector in accordance with a select signal.

7. (Original) A decoder for demodulating address information using a wobble signal, the decoder comprising:

a digital PLL circuit for generating a first clock signal and synchronizing the first clock signal with the wobble signal based on a difference between the phase of the wobble signal and the phase of the first clock signal;

an analog PLL circuit for generating a second clock signal and synchronizing the second clock signal with the wobble signal based on a difference between the phase of the wobble signal and the phase of the second clock signal;

a detection circuit for comparing the wobble signal and the second clock signal, detecting whether the second clock signal is synchronized with the wobble signal, and generating an active select signal when the second clock signal is synchronized with the wobble signal; and

a demodulator, connected to the digital PLL circuit, the analog PLL circuit, and the detection circuit, for sampling the wobble signal using the first clock signal to demodulate the address information when the select signal is inactive and for sampling the wobble signal using the second clock signal to demodulate the address information when the select signal is active.

8. (Original) The decoder as claimed in claim 7, wherein the demodulator includes:

a first phase detector, connected to the digital PLL circuit, for detecting a phase inversion of the wobble signal based on the first clock signal and generating a first phase detection signal;

a second phase detector, connected to the analog PLL circuit, for detecting a phase inversion of the wobble signal based on the second clock signal and generating a second phase detection signal;

a selector, connected to the first and second phase detectors and the detection circuit, for selecting the first phase detection signal in response to the inactive select signal and selecting the second phase detection signal in response to the active select signal; and

a demodulator circuit, connected to the selector, for demodulating the address information using the selected phase detection signal.

9. (Currently Amended) The decoder as claimed in claim 1, wherein the analog PLL circuit generates the second [[~~elick~~]] clock signal as a reference signal.

10. (Currently Amended) The decoder as claimed in claim 7, wherein the analog PLL circuit generates the second [[~~elick~~]] clock signal as a reference signal.

11. (New) The decoder as claims in claim 1, wherein the demodulator samples the wobble signal using the first clock signal until the second clock signal is synchronized with the wobble signal and samples the wobble signal using the second clock signal after the second clock signal is synchronized with the wobble signal.